



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/799,292

03/12/2004

Kyoung-woo Lee

SAM-0560

8218

7590

01/05/2007

Steven M. Mills  
MILLS & ONELLO LLP  
Suite 605  
Eleven Beacon Street  
Boston, MA 02108

EXAMINER

SARKAR, ASOK K

ART UNIT

PAPER NUMBER

2891

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
--	-----------	---------------

3 MONTHS

01/05/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/799,292	<b>Applicant(s)</b> LEE ET AL.	
	<b>Examiner</b> Asok K. Sarkar	<b>Art Unit</b> 2891	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 November 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 16-39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 34-36 is/are allowed.
- 6) ☒ Claim(s) 16,22,27,30,31 and 37-39 is/are rejected.
- 7) ☒ Claim(s) 17-21,23-26,28,29,32 and 33 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 16 – 39 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 16, 22, 27, 30 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshitomi, US 6,740,974.

Regarding claim 16, Yoshitomi teaches a dual damascene interconnection structure with a metal – insulator – metal capacitor, the structure comprising:

- a via – level intermetal dielectric 21 and a trench – level intermetal dielectric 22 which are sequentially stacked on a substrate;
- a dual damascene interconnection 27C formed in the via – level intermetal dielectric and the trench – level intermetal dielectric including a line trench extending through the trench – level intermetal dielectric to the via – level intermetal dielectric; and

- a metal – insulator – metal capacitor 20 formed between the via – level intermetal dielectric and the trench – level intermetal dielectric to include a lower electrode 16, a dielectric layer 17, and an upper electrode 18, the dual damascene interconnection being substantially electrically isolated from the metal-insulator-metal capacitor; and
- an upper metal interconnection 27b formed on and connected to the upper electrode with reference to Figs. 7 and 13 and corresponding text under columns 2 – 6.

Regarding claim 22, Yoshitomi teaches the upper electrode 18 is patterned to have a smaller area than that of each of the lower electrode 16 and the capacitor dielectric layer 17 with reference to Figs 7 and 13.

Regarding claim 27, Yoshitomi teaches a dual damascene interconnection is formed with Cu in column 4, lines 5 – 7.

Regarding claim 30, Yoshitomi teaches the dual damascene interconnection further includes a via hole formed in the via – level intermetal dielectric 21 with reference to Fig. 6.

Regarding claim 31, Yoshitomi teaches an upper metal interconnection positioned in a trench, wherein the trench is formed in the trench – level intermetal dielectric 22 to expose the upper electrode with reference to Figs 7 and 13.

4. Claims 37 – 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Ogawa, US 2003/0012117.

Regarding claim 37, Ogawa teaches a dual damascene interconnection

structure with a metal – insulator – metal capacitor, the structure comprising:

- a via – level intermetal dielectric 22 and a trench – level intermetal dielectric 41 which are sequentially stacked on a substrate 10;
- a dual damascene interconnection 42/30C formed in the via - level intermetal dielectric and the trench – level intermetal dielectric;
- a metal – insulator – metal MC capacitor formed between the via – level intermetal dielectric and the trench – level intermetal dielectric to include a lower electrode 33b, a dielectric layer 34 , and an upper electrode 35; and
- a first lower metal interconnection 21b formed between the substrate and the via – level intermetal dielectric, herein the lower electrode 33b is directly connected to the first lower metal interconnection 21b with reference to Fig.1A.

Regarding claim 38, Ogawa teaches a via 30b formed in the via – level intermetal dielectric 22, wherein the lower electrode 33b is located on the via with reference to Fig. 1A.

Regarding claim 39, Ogawa teaches the via and the lower electrode are united together as a single body with reference to Fig. 1A.

#### ***Allowable Subject Matter***

5. Claims 17 – 21, 23 – 26, 28, 29, 32 and 33 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 34 – 36 are allowed.

#### ***Conclusion***

Art Unit: 2891

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2891

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Asok K. Sarkar  
December 21, 2006

Primary Examiner